



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/692,606	10/19/2000	Jack Oon Chu	YOR920000334US1	7913

7590 07/31/2003
Robert M. Trepp
IBM CORPORATION
Intellectual Property Law Dept.
P.O. BOX 218
Yorktown Heights, NY 10598

EXAMINER

KIELIN, ERIK J

ART UNIT PAPER NUMBER

2813

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/692,606

Applicant(s)

CHU ET AL.

Examiner

Erik Kielin

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) 2-5, 7, 8, 11-17 and 24-42 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 6, 9, 10 and 18-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 October 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4, 6.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of invention I, species Ia, claims (1, 6, 9, 10, and 18-23) in Paper No. 3 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claims 2-5, 7, 8, 11-17, 24-30, and 31-42 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected species, there being no allowable generic or linking claim.

Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states; "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered. In the instant case, US Patent Applications 09/675840 and 09/675841 have not been considered because no copies have been provided, as required.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, (1) the "bonding said top surface of said relaxed Si_{1-y}Ge_y layer... to the top surface of said second substrate," as recited in claim 1,

Art Unit: 2813

lines 11-12, and (2) the "intermediate agent layer, must be shown or the feature(s) canceled from the claim(s). *No new matter should be entered.*

Regarding claim 1, the figures presently show that the top surface 42 of encapsulation layer 40 is bonded to the top surface 90 of the second substrate 80 -- not the relaxed SiGe layer 30.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

on p. 2, lines 23 and 24, replace "um" with -- μ m-- for accurate nomenclature;

on p. 3, lines 2 and 4, replace "um" with -- μ m-- for accurate nomenclature;

on p. 4, line 21, replace "remaaining" with --remaining-- for correct spelling;

on p. 6, lines 7-8, replace "Serial no. 09/107567 filed Jun. 29, 1998" with --U.S. Patent No. 6,147,009-- to update information;

on p. 6, lines 9, 22, and 27, remove the parenthetical docket numbers;

on p. 7, line 4, replace "tot he" with --to the-- for correct spelling;

on p. 7, lines 6, 19, and 21, replace "um" with -- μ m-- for accurate nomenclature; and

on p. 8, line 11, replace "heterostrcuture" with --heterostructure-- for correct spelling.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 6, 19, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim 1 recites the limitation "said top surface" in line 11. There is insufficient antecedent basis for this limitation in the claim. This rejection could be overcome by replacing the word "top" with "smoothed."

8. Claim 6 recites the limitation "said low-defect relaxed Si_{1-y}Ge_y layer" in line 1. There is insufficient antecedent basis for this limitation in the claim. This rejection could be overcome by removing the additional limitation "low-defect."

9. Claim 19 recites the limitation "said smoothed top surface of said first Si_{1-y}Ge_y relaxed layer" in line 1. There is insufficient antecedent basis for this limitation in the claim. This rejection could be overcome by removing the words "top" and "first."

10. Claim 21 is considered indefinite because of the mixed phraseology "*from the group consisting of* furnace anneal *and/or* rapid thermal anneal." (Emphasis added.) It cannot be determined whether either of the methods or both is claimed. Examiner suggests removing "/or" to be consistent with the phrase "from the group consisting of."

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 9, 10, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,521,041 B2 (**Wu** et al.) in view of US 6,328,796 B1 (**Kub** et al.).

Wu discloses a method of preparing a relaxed SiGe layer on an insulator and a SiGe/Si heterostructure comprising the steps of

forming a graded $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer **1004** on a first single crystalline semiconductor substrate **1002** (col. 1, lines 9-10; Fig. 10);

forming a relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **1006** (col. 13, lines 63-64; col. 8, lines 40-48) over said graded $\text{Si}_{1-x}\text{Ge}_x$ layer;

selecting a second substrate **1010**, said second substrate with or without an insulator **1012**; and

bonding said top surface of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer on said first substrate to the top surface of said second substrate, said step of bonding including the step of annealing to form sufficiently strong bonds across the bonding interface to form a single mechanical structure (Fig. 10). (See also col. 13, line 63 to col. 14, line 23.)

Further regarding claim 1 and claim 10 **Wu** does not indicate whether or not the surface of the relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **1006** is smoothed to provide a surface roughness in the range from about 0.3 nm to about 1 nm root mean square (RMS) using chemical mechanical

Art Unit: 2813

planarization (CMP) --as further limited by instant claim 10-- prior to bonding, or that the second substrate **1010** with or without an insulator **1012** has a surface roughness in the range from about 0.3 nm to about 1 nm RMS prior to bonding.

Kub teaches that in order to obtain direct bonding between substrates, that the bonding surfaces must have a RMS surface roughness of less than 1 nm and can be obtained by polishing (col. 4, lines 4-8) and that such polishing is known in the art to be chemical mechanical polishing (col. 3, lines 30-32).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to smooth the relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **1006** of Wu using CMP and to provide a surface roughness on the bonding surface of the second substrate **1012** each of less than 1 nm, in order to ensure bonding, as taught by **Kub**.

Regarding claim 9, **Wu** discloses that the first substrate **1002** is selected from the group consisting of Si, SiGe, SiGeC, SiC, GaAs, or InP.

Regarding claim 18, **Wu** discloses that the second substrate **1010** is selected from the group consisting of Si, SiGe, SiGeC, SiC, GaAs, InP, sapphire, glass, quartz, LiNbO_3 , and PLZT.

Regarding claim 19, **Wu** discloses that said the top surface of said first $\text{Si}_{1-y}\text{Ge}_y$ relaxed layer **1006** on said first substrate **1002** is brought into intimate contact with said top surface of an insulator layer **1012** on said second substrate **1010**.

Regarding claim 20, **Wu** does not teach using an intermediate agent layer selected from the group consisting of Ge, Al, W, Co, and Ti may be used to enhance the bonding interface.

Art Unit: 2813

Kub also teaches that it is known in the art to use an agent layer such as metals to aid the bonding between substrates (col. 4, lines 13-37).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use an agent layer of a metal or germanium to enhance the bonding of the substrates in **Wu**, in order to aid the bonding of the substrates, as taught by **Kub**.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Wu** in view of **Kub** as applied to claim 1 above, and further in view of US 5,906,951 (**Chu et al.**).

The prior art of **Wu**, as explained above, discloses each of the claimed features except for providing the thickness low-defect relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer on said second substrate to be in the range from about 50 nm to about 1000 nm as determined by the layer structure formed on said first substrate.

Chu teaches a very similar method to that in **Wu** of using a relaxed silicon-germanium layer as an etch stop and teaches that the thickness may be from 200 nm to 1000 nm (col. 2, lines 61-67; Fig. 3).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the thickness of 200 nm to 1000 nm as the relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer of **Wu**, because **Wu** is silent to the thickness, such that one of ordinary skill must determine the appropriate thickness, and using a known thickness for an etch stop in a similar method would dramatically reduce the experimentation required to determine the proper thickness. With this in mind, the choice of thickness range is *prima facie* obvious without showing that the claimed range achieves unexpected results relative to the prior art range. See *In re Woodruff*, 16 USPQ2d 1935, 1937

Art Unit: 2813

(Fed. Cir. 1990). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

4. Claims 1, 9, 10, 19, and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,573,126 B2 (**Cheng et al.**) in view of **Kub '796**.

Cheng discloses a method of preparing a relaxed SiGe layer on an insulator and a SiGe/Si heterostructure comprising the steps of

forming a graded $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer **102** on a first single crystalline semiconductor substrate **100** (Fig. 1A);

forming a relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **104** over said graded $\text{Si}_{1-x}\text{Ge}_x$ layer (Fig. 1A);

smoothing the surface of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **104** to provide a surface roughness in the range from about 0.3 nm to about 1 nm root mean square (RMS) using CMP (col. 4, last paragraph) --as further limited by instant claim 10;

selecting a second substrate **108**, said second substrate with or without an insulator **106** (Fig. 1B); and

bonding said top surface of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer on said first substrate to the top surface of said second substrate, said step of bonding including the step of annealing to form sufficiently strong bonds across the bonding interface to form a single mechanical structure (Fig. 1B). (See also col. 3, lines 28-37; col. 4, lines 20-34; paragraph bridging cols. 4 and 5; col. 5, lines 4-16.)

Cheng does not indicate whether or not the second substrate **108** with or without an insulator **106** has a surface roughness in the range from about 0.3 nm to about 1 nm RMS prior to bonding.

Kub '796 teaches that in order to obtain direct bonding between substrates, that the bonding surfaces must have a RMS surface roughness of less than 1 nm and can be obtained by polishing (col. 4, lines 4-8).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to provide a surface roughness on the bonding surface of the second substrate **106** of less than 1 nm, in order to ensure bonding, as taught by **Kub '796**.

Regarding claim 21, **Cheng** discloses that the step of annealing includes thermal treatment cycles to form a strong bond at said bonded interface, said thermal treatment selected from the group consisting of furnace anneal and/or rapid thermal anneal (RTA) (col. 4, lines 20-34; col. 5, lines 51-53).

Regarding claim 23, **Cheng** discloses that the annealing step includes annealing at 600 °C and 850 °C (col. 4, lines 20-34).

5. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Cheng** in view of **Kub '796** as applied to claims 1 and 21 above, and further in view of US 6,153,495 (**Kub et al.**).

The prior art of **Cheng** in view of **Kub '796**, as explained above, discloses each of the claimed features except for indicating what the annealing ambient is or more specifically that the ambient is selected from the group consisting of air, N₂ and Ar.

Art Unit: 2813

Kub '495 teaches that the bonding ambient for bonding a semiconductor layer to an oxide layer may include nitrogen (N₂) and argon (Ar) (col. 6, lines 23-38).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use an anneal ambient selected from the group consisting of N₂ and Ar, because **Cheng** is silent to the annealing ambient such that one of ordinary skill would use an ambient known for successful wafer bonding, such as that taught in **Kub'495**.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,103,597 (**Aspar** et al.) teaches that it is known in the art, that the bonding surface, surface roughness must be less than 0.5 nm to ensure proper bonding, and that such smoothing to reduce the roughness to required levels may be obtained using CMP (col. 6, lines 24-36).

US 5,013,681 (**Godbey** et al.) teaches the use of SiGe as an etch stop layer (col. 3, lines 39-29).

US 6,323,108 B1 (**Kub** et al.) teaches wafer bonding at <800 °C and the use of SiGe as an etch stop (col. 7, lines 11-25 and lines 50-63).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

Art Unit: 2813

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Erik Kielin
July 15, 2003